WHAT IS CLAIMED IS:

1. A computer system, comprising:

the central processing unit operably coupled to the memory;

and

an integrated circuit board, the integrated circuit board comprising:

a first voltage plane;

a second voltage plane, wherein the second voltage plane is parallel to the first voltage plane;

a core layer operably disposed between the first voltage plane and second voltage plane;

a dielectric layer operably disposed on a portion of the first voltage plane;

a ground pad, wherein the ground pad is operably disposed on the dielectric layer;

a capacitor, wherein the capacitor is operably disposed on the ground pad;

a voltage pad, the voltage pad electrically coupled to the first voltage plane;

and

a via, the via electrically coupling the ground pad to the second voltage plane.

2. The computer system as recited in claim 1, wherein the capacitor is a surface mounted capacitor.

3. The computer system as recited in claim 1, wherein the capacitor is a bypass capacitor.

4. The computer system as recited in claim 1, wherein the number of via is less than or equal to six and not equal to the number of electrical connections from the voltage pad to the first voltage plane.

5. The computer system as recited in claim 1, wherein the operating frequency of the capacitor is greater than or equal to 100 Mhz.

6. The computer system as recited in claim 5, wherein the operating frequency of the capacitor is less than or equal to 800 Mhz.

7. The computer system as recited in claim 1, wherein the ground pad has a length and a width, wherein the ground pad is a minimum of 0.1 inches in width.

8. The computer system as recited in claim 7, wherein the ground pad is a minimum of 0.1 inches in length.

9. An integrated circuit board designed to reduce the inductance of a capacitor, comprising:

a first voltage plane;

a second voltage plane, wherein the second voltage plane is parallel to the first voltage plane;

a core layer operably disposed between the first voltage plane and the second voltage plane;

a dielectric layer, wherein the dielectric layer is operably disposed on a portion of the first voltage plane;

a ground pad, wherein the ground pad is operably disposed on the dielectric layer;

a trace, the trace electrically coupled to the ground pad;

a capacitor, wherein the capacitor is operably disposed on the ground pad;

a voltage pad, the voltage pad electrically coupled to the first voltage plane; and

a plurality of via, the plurality of via electrically coupling the trace to the second voltage plane, the number of via greater than the number of electrical couplings between the voltage pad and the first voltage plane.

10. The integrated circuit board as recited in claim 9, wherein the capacitor is a bypass capacitor.

11. The integrated circuit board as recited in claim 9, wherein the capacitor is a surface mounted capacitor.

12. The integrated circuit board as recited in claim 9, wherein the number of via is less than or equal to six and not equal to the number of electrical couplings from the voltage pad to the voltage plane.

13. The integrated circuit board as recited in claim 9, wherein the operating frequency of the capacitor is greater than or equal to 100 Mhz.

14. The integrated circuit board as recited in claim 13, wherein the operating frequency of the capacitor is less than or equal to 800 Mhz.

15. The integrated circuit board as recited in claim 9, further comprising:

a ground pad, wherein the ground pad has a width and a length, wherein the minimum length of the ground pad is 0.1 inch.

16. The integrated circuit board as recited in claim 15, wherein the ground pad has a width and a length, wherein the minimum width of the ground pad is 0.1 inch.

17. A method of designing an integrated circuit board to reduce the inductance of a capacitor, comprising:

providing a first voltage plane;

providing a second voltage plane, wherein the second voltage plane is parallel to the first voltage plane;

providing a core layer, the core layer operably disposed between the first voltage plane and the second voltage plane;

providing a dielectric layer, wherein the dielectric layer is operably disposed on a portion of the first voltage plane;

providing a ground pad, the ground pad operatively disposed on the dielectric layer;

providing a capacitor, the capacitor operably disposed on the ground pad;

providing a voltage pad, the voltage pad electrically coupled to the first voltage plane; and

providing a via, the via electrically coupling the ground pad to the second voltage plane.

18. The method of designing an integrated circuit board as recited in claim 17, wherein the capacitor is a bypass capacitor.

19. The method of designing an integrated circuit as recited in claim 17, wherein the capacitor is a surface mounted capacitor.

20. The method of designing an integrated circuit as recited in claim 17, wherein the number of via are less than or equal to six and not equal to the number of electrical couplings from the voltage pad to the voltage plane.

21. The method of designing an integrated circuit board as recited in claim 17, wherein the capacitor operates at a frequency greater than or equal to 100 Mhz.

22. The method of designing an integrated circuit board as recited in claim 21, wherein the capacitor operates at a frequency less than or equal to 800 Mhz.

23. The method of designing an integrated circuit board as recited in claim 17, wherein the ground pad is a rectangular shape, the ground pad having a minimum length of 0.10 inch.

24. The method of designing an integrated circuit board as recited in claim 23, wherein the ground pad is a minimum width of 0.10 inch.

25. A method of designing an integrated circuit board to reduce the inductance of a capacitor, comprising:

providing a first voltage plane;

providing a second voltage plane, wherein the second voltage plane is parallel to the first voltage plane;

providing a core layer, the core layer operably disposed between the first voltage plane and the second voltage plane;

providing a dielectric layer, wherein the dielectric layer is operably disposed on a portion of the first voltage plane;

providing a ground pad, the ground pad operatively disposed on the dielectric layer;

providing a trace, the trace electrically coupled to the ground pad;

providing a capacitor, the capacitor operably disposed on the ground pad;

providing a voltage pad, the voltage pad electrically coupled to the first voltage plane; and

providing a via, the via electrically coupling the trace to the second voltage plane, the number of via less than six and the number of via greater than the number of electrical couplings between the voltage pad and the first voltage plane.

26. The method of designing an integrated circuit board as recited in claim 25, wherein the capacitor is a bypass capacitor.

27. The method of designing an integrated circuit as recited in claim 26, wherein the capacitor is a surface mounted capacitor.

28. The method of designing an integrated circuit board as recited in claim 25, wherein the capacitor operates at a frequency greater than or equal to 100 Mhz.

29. The method of designing an integrated circuit board as recited in claim 28, wherein the capacitor operates at a frequency less than or equal to 800 Mhz.

30. The method of designing an integrated circuit board as recited in claim 25, wherein the ground pad has a width and a length, the ground pad having a minimum length of 0.10 inch.

31. The method of designing an integrated circuit board as recited in claim 30, wherein the ground pad has a minimum width of 0.10 inch.